WHAT IS CLAIMED IS:

1. A system for implementing an electronic device, comprising:

a transmission source configured to provide priority information for use by said electronic device;

a memory device coupled to said transmission source and configured for storing said priority information; and

a processor coupled to said memory device for utilizing said priority information from said memory device.

2. The system of claim 1 wherein said priority information includes isochronous data for performing a time-sensitive isochronous process.

3. The system of claim 1 wherein said memory device and said processor are coupled to one of a computer device, a set-top box, a digital television device, and a consumer electronic device.

4. The system of claim 1 wherein said transmission source includes one of an input/output bus, a computer device, a network node, or an audio-video device.

5. The system of claim 1 wherein said electronic device is part of an electronic network that is implemented according to an IEEE 1394 serial bus standard.

6. The system of claim 2 wherein said memory device includes an isochronous memory that is reserved for storing only said isochronous data, said isochronous memory being inaccessible to any non-isochronous processes for storing non-isochronous data, said isochronous memory being reconfigurable by a memory manager and a memory controller into separate memory channels that are mapped to isochronous processes.

7. The system of claim 2 wherein said memory device comprises an isochronous memory, said isochronous memory including a memory controller, one or more memory channels, and memory registers.

8. The system of claim 7 wherein said memory registers include at least one of a total channels field, an allocated channels field, a total memory field, an allocated memory field, and one or more channel registers.

9. The system of claim 8 wherein said channel registers include at least one of a process identifier field and a required memory field.

10. The system of claim 8 wherein a memory manager initiates a channel setup procedure after receiving a channel setup request from a requesting entity to configure a new memory channel for an isochronous process, said channel setup request including at least one of a data transfer size, an isochronous process identifier, a transmission bus channel number for mapping to a corresponding isochronous memory channel number, and a transfer direction indicator.

11. The system of claim 10 wherein said memory manager allocates said new memory channel only after determining that said new memory channel is available by analyzing said total channels field and said allocated channels field in said memory registers.

12. The system of claim 10 wherein said memory manager allocates said new memory channel only after determining that a sufficient memory space is available for said new memory channel by analyzing said total memory field and said allocated memory field in said memory registers, and said required memory field in a corresponding channel register.

13. The system of claim 10 wherein said memory manager transmits a new channel allocation message to said memory controller, said memory controller responsively reconfiguring said isochronous memory to include said new memory channel.

14. The system of claim 13 wherein said memory manager returns a setup completion message and a memory channel number to said requesting entity, said memory manager also updating said memory registers to account for said new memory channel.

15. The system of claim 7 wherein said memory controller begins a data transfer operation in response to detecting an isochronous indicator.

16. The system of claim 15 wherein said memory controller determines that said data transfer operation is a send operation to an input-output bus, and responsively invokes send logic that arbitrates for access to said system bus and then transmits said isochronous data from said isochronous memory to said input-output bus over said system bus.

17. The system of claim 15 wherein said memory controller determines that said data transfer operation is a receive operation from an input-output bus, responsively utilizes a mapping technique to identify an allocated memory channel in said isochronous memory, and then transfers said isochronous data from said input-output bus over said system bus into said allocated isochronous channel.

18. The system of claim 7 wherein said processor begins a data transfer operation over said system bus by sending a data transfer request to said memory controller in said isochronous memory, said data transfer request including a mode bit to indicate one of a FIFO mode and a random-access mode.

19. The system of claim 18 wherein said processor performs a read operation from said isochronous memory, said read operation being performed sequentially in said FIFO mode, and said read operation being performed using a memory location address in said random-access mode.

20. The system of claim 18 wherein said processor performs a write operation to said isochronous memory, said write operation being performed sequentially in said FIFO mode, and said write operation being performed using a memory location address in said random-access mode.

21. A method for implementing an electronic device, comprising the steps of:

providing priority information from a transmission source for use by said electronic device;

configuring a memory device to store said priority information; and

accessing said priority information from said memory device by using a processor.

22. The method of claim 21 wherein said priority information includes isochronous data for performing a time-sensitive isochronous process.

23. The method of claim 21 wherein said memory device and said processor are coupled to one of a computer device, a set-top box, a digital television device, and a consumer electronic device.

24. The method of claim 21 wherein said transmission source includes one of an input/output bus, a computer device, a network node, or an audio-video device.

25. The method of claim 21 wherein said electronic device is part of an electronic network that is implemented according to an IEEE 1394 serial bus standard.

26. The method of claim 22 wherein said memory device includes an isochronous memory that is reserved for storing only said isochronous data, said isochronous memory being inaccessible to any non-isochronous processes for storing non-isochronous data, said isochronous memory being reconfigurable by a memory manager and a memory controller into separate memory channels that are mapped to isochronous processes.

27. The method of claim 22 wherein said memory device comprises an isochronous memory, said isochronous memory including a memory controller, one or more memory channels, and memory registers.

28. The method of claim 27 wherein said memory registers include at least one of a total channels field, an allocated channels field, a total memory field, an allocated memory field, and one or more channel registers.

29. The method of claim 28 wherein said channel registers include at least one of a process identifier field and a required memory field.

30. The method of claim 28 wherein a memory manager initiates a channel setup procedure after receiving a channel setup request from a requesting entity to configure a new memory channel for an isochronous process, said channel setup request including at least one of a data transfer size, an isochronous process identifier, a transmission bus channel number for mapping to a corresponding isochronous memory channel number, and a transfer direction indicator.

31. The method of claim 30 wherein said memory manager allocates said new memory channel only after determining that said new memory channel is available by analyzing said total channels field and said allocated channels field in said memory registers.

32. The method of claim 30 wherein said memory manager allocates said new memory channel only after determining that a sufficient memory space is available for said new memory channel by analyzing said total memory field and said allocated memory field in said memory registers, and said required memory field in a corresponding channel register.

33. The method of claim 30 wherein said memory manager transmits a new channel allocation message to said memory controller, said memory controller responsively reconfiguring said isochronous memory to include said new memory channel.

34. The method of claim 33 wherein said memory manager returns a setup completion message and a memory channel number to said requesting entity, said memory manager also updating said memory registers to account for said new memory channel.

35. The method of claim 27 wherein said memory controller begins a data transfer operation in response to detecting an isochronous indicator.

36. The method of claim 35 wherein said memory controller determines that said data transfer operation is a send operation to an input-output bus, and responsively invokes send logic that arbitrates for access to said system bus and then transmits said isochronous data from said isochronous memory to said input-output bus over said system bus.

37. The method of claim 35 wherein said memory controller determines that said data transfer operation is a receive operation from an input-output bus, responsively utilizes a mapping technique to identify an allocated memory channel in said isochronous memory, and then transfers said isochronous data from said input-output bus over system bus into said allocated isochronous channel.

38. The method of claim 27 wherein said processor begins a data transfer operation over said system bus by sending a data transfer request to said memory controller in said isochronous memory, said data transfer request including a mode bit to indicate one of a FIFO mode and a random-access mode.

39. The method of claim 38 wherein said processor performs a read operation from said isochronous memory, said read operation being performed sequentially in said FIFO mode, and said read operation being performed using a memory location address in said random-access mode.

40. The method of claim 38 wherein said processor performs a write operation to said isochronous memory, said write operation being performed sequentially in said FIFO mode, and said write operation being performed using a memory location address in said random-access mode.

41. The method of claim 21 wherein said memory device includes a random access memory.

42. The method of claim 41 wherein said random access memory may be configured to include isochronous memory which operates as a first-in-first-out memory.

43. The method of claim 21 wherein said memory device, said transmission source, and said processor communicate bi-directionally over a system bus.

44. The method of claim 43 wherein said system bus includes an asynchronous bus for transmitting asynchronous information, and an isochronous bus for transmitting isochronous information.

45. The method of claim 44 wherein said system bus comprises a control bus which includes a transfer indicator, said transfer indicator including one of an asynchronous indicator and an isochronous indicator.

46. The method of claim 45 wherein said isochronous indicator designates a transfer of said isochronous information for storing into an assigned memory channel in an isochronous memory by reference to an associated channel number.

47. The method of claim 44 wherein said isochronous bus comprises a write bus for performing a write operation to transfer said isochronous information into an isochronous memory, and also comprises a read bus for performing a read operation to transfer said isochronous information from said isochronous memory.

48. The method of claim 47 wherein said write operation and said read operation occur concurrently.

49. The method of claim 48 wherein a transfer arbiter separately limits access to one or more of said write bus and said read bus by allowing a respective current transfer operation to complete before authorizing a respective subsequent corresponding transfer operation to begin.

50. A computer-readable medium comprising program instructions for implementing an electronic device by performing the steps of:

providing priority information from a transmission source for use by said electronic device;

configuring a memory device to store said priority information; and

accessing said priority information from said memory device by using a processor.

51. A system for implementing an electronic device, comprising:

means for providing priority information from a transmission source for use by said electronic device;

means for configuring a memory device to store said priority information; and

means for accessing said priority information from said memory device by using a processor.